REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for careful review of this application.

I. Election of Claims

Applicant confirms the election of Group I, which includes claims 1-6 and 18-27 and relates to a phase detector, for continued prosecution without traverse. Non-elected claims 7-17 have been withdrawn in this reply.

II. Objections to Claims

Claim 2 was objected to as being redundant. Claim 2 has been canceled by this reply without prejudice or disclaimer, rendering the objection to the claim moot. Accordingly, withdrawal of this objection is respectfully requested.

Claims 20-22 were objected to under 37 C.F.R. 1.75(c) as being of improper dependent form for failing to further limit the subject matter of the previous claim. Claims 20-22 have been canceled by this reply without prejudice or disclaimer, rendering the objection to claims 20-22 moot. Accordingly, withdrawal of this objection is respectfully requested.

III. Rejections Under 35 U.S.C. § 102

U.S. PATENT NO. 4,122,405

Claims 1, 2, 18, and 19 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,122,405 ("Tietz"). Claim 2 has been canceled by this reply without prejudice or disclaimer, rendering the rejection of the claim moot. Claim 19 has been amended to clarify the present invention recited. The amendments are fully supported by the specification, *e.g.*, Figures 3-4, and the accompanying description. To the extent that the rejection still applies to the remaining claims, the rejection is respectfully traversed.

Independent claim 1 recites a computer system that comprises a phase locked loop and a lock detect indicator. The phase locked loop includes a phase-frequency detector that inputs a system clock and generates a chip clock, where the phase-frequency detector generates pulses on a first signal and a second signal dependent on a relationship between the system clock

and the chip clock. Further, using the first and second signals, the lock detect indicator determines whether the phase locked loop is out of lock. Similarly, independent claim 18 recites an integrated circuit that comprises generating means, detecting means, and indicating means. The generating means uses a first signal and a second signal to maintain a relationship between the chip clock and the system clock, the detecting means uses the first and second signals to determine whether the generating means is out of lock, and the indicating means indicates whether the generating means is out of lock.

As amended, independent claim 19 recites a method for detecting whether a phase locked loop is out of lock, where the method comprises generating a first signal and a second signal based on a relationship between a system clock and a chip clock used in the phase locked loop, determining whether a pulse of the first signal or the second signal is greater than a predetermined width, generating a pulse on a first lock signal based on the determination, and dynamically generating a pulse on a lock status signal dependent on the pulse on the first lock signal. Further, the first and second signals are generated using a phase-frequency detector of the phase locked loop.

In the present application, Figures 2 and 3 show that a phase locked loop **40** includes a phase frequency detector **44**, a charge pump/filter **46**, and a voltage controlled oscillator **48**. Using a system clock, the phase-frequency detector **44** generates a first signal (**fast_pulse**) and a second signal (**slow_pulse**). Depending on the values of the first and second signals, the charge/pump filter **46** dumps/removes charge to/from a voltage signal that the voltage controlled oscillator **48** uses to generate a chip clock (page 2, paras. 4-5). Thus, as is shown in the present application, a phase locked loop requires a phase-frequency detector **44**, a charge/pump filter **46**, and a voltage controlled oscillator **48** in order to generate the chip clock.

With regard to claim 1, the Examiner asserts that Figure 1 of Tietz teaches a circuit comprising a lock detect indicator (**12, 14, 16**) and an inherent phase locked loop having a phase-frequency detector **10**, where the phase frequency detector **10** inputs a system clock **18** and generates a chip clock **20**. However, as is described above, a phase locked loop requires requires a phase-frequency detector, a charge/pump filter, and a voltage controlled oscillator in order to generate a chip clock. Tietz discloses neither a charge/pump filter nor a voltage controlled

oscillator. Accordingly, Tietz does not disclose a phase locked loop for generating a first signal, a second signal, and a chip clock as required by claim 1 of the present application.

Further, as is described in Tietz, element **10** is a coupled to a phase locked loop, rather than included as a part of an inherent phase locked loop (Tietz, col. 2, lines 24-25). Thus, in contrast to the present invention, element **10** is not used in a phase locked loop to generate a chip clock, but rather, is included in the circuitry that receives the chip clock outputted by the phase locked loop. Thus, element **10** is not a phase-frequency detector included in a phase locked loop as required by claim 1, but rather, a phase comparator **10** that receives signals generated by the phase locked loop. Accordingly, Tietz does not disclose a phase-frequency detector included in a phase locked loop as required by claim 1 of the present application. Therefore, withdrawal of the § 102(b) rejection is respectfully requested. Claims 3-6, which depend from claim 1, are patentable for at least the same reasons. Likewise, Tietz fails to teach or suggest generating means for generating a chip clock signal based on a system clock signal as claimed in claim 18 of the present invention. Therefore, withdrawal of the § 102(b) rejection is respectfully requested.

Similarly, Tietz fails to teach or suggest a method for detecting whether a phase locked loop is out of lock as claimed in claim 19, where the method comprises a step for generating a first signal and a second signal based on a relationship between a system clock and a chip clock used in the phase locked loop, and where the first signal and the second signal are generated by a phase-frequency detector included in the phase locked loop. Therefore, withdrawal of the § 102(b) rejection is respectfully requested. Claims 23-27, which depend from claim 19, are patentable for at least the same reasons.

U.S. PATENT NO. 6,177,842

Claims 1, 6, 18, 19, and 25 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,177,842 ("Ahn"). This rejection is respectfully traversed.

The Examiner asserts that Figures 1-2B of Ahn teach a circuit, and a method of use thereof, that comprises a lock detect indicator **103** and an inherent phase locked loop having a phase-frequency detector **101**, where the phase-frequency detector **101** generates pulses on a first signal (lockdet) and a second signal (lockdetb) dependent on a relationship between a system

clock and a chip clock, and where the lock detect indicator **103** uses the first and second signals to determine whether the phase locked loop is out of lock.

However, as is described for Figure 1 of Ahn, a lock detect indicator circuit **100** includes a phase detection circuit **101** and a phase lock indication circuit **103**, where the phase detection circuit **101** is configured to receive a first signal and a second signal and to determine whether the first and second signals are in phase, *i.e.*, in lock, and the phase lock indication circuit **103** is configured to output the lock status detected by the phase detection circuit **101** (col. 3, line 56 – col. 4, line 13). Thus, element **101** and **103** do not respectively represent phase-frequency detector of an inherent phase locked loop and a lock detect indicator circuit, but, rather, components of a lock detect indicator circuit. Accordingly, Ahn does not disclose a phase locked loop having a phase-frequency detector as required by claim 1 of the present application. Therefore, withdrawal of the § 102(e) rejection is respectfully requested. Claims 3-6, which depend from claim 1, are patentable for at least the same reasons. Likewise, Ahn fails to teach or suggest generating means for generating a chip clock signal based on a system clock signal as claimed in claim 18 of the present invention. Therefore, withdrawal of the § 102(e) rejection is respectfully requested.

Similarly, Ahn fails to teach or suggest a method for detecting whether a phase locked loop is out of lock as claimed in claim 19, where the method comprises a step for generating a first signal and a second signal based on a relationship between a system clock and a chip clock used in the phase locked loop, and where the first signal and the second signal are generated by a phase-frequency detector included in the phase locked loop. Therefore, withdrawal of the § 102(e) rejection is respectfully requested. Claims 23-27, which depend from claim 19, are patentable for at least the same reasons.

IV. Rejections Under 35 U.S.C. § 103

Claims 3-5, 23, 24, 26, and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tietz. This rejection is respectfully traversed. As discussed above, Tietz fails to show or suggest the present invention as claimed in the independent claims. Therefore, the claims cannot be rendered obvious. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

V. Conclusion

Applicant believes this reply to be fully responsive to all outstanding issues and place this application in condition for allowance. If this belief is incorrect, or other issues arise, do not hesitate to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.139001).

Respectfully submitted,

Date: 3/5/08

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